AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus comprising:

a variable speed bus, the variable speed bus initialized with a first clock frequency;

a first unit coupled to the variable speed bus, the first unit having a first rate of requests to access the variable speed bus;

a second unit coupled to the variable speed bus, the second unit having a second rate of requests to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on the first access rate or the second access request rate, ~~wherein~~ the arbitration and bus clock control unit ~~is further~~ being modified to track a rate of request of the first and second units to access the variable speed bus, the arbitration and bus clock control unit ~~is~~ being further modified to recognize when there are no incoming requests and a percentage of arbitration slots that are being used, and to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request, wherein the adjusting of the clock frequency includes lowering the clock frequency to a lowest level necessary in accordance with the recognition of no incoming requests and the percentage of the arbitration slots being used and further in accordance

with a historical average utilization including statistical data relating to sustained bandwidth needs such that the clock frequency of the variable speed bus is automatically adjusted depending on one or more of the rate of request, the percentage of arbitration slots being used, and the historical average utilization relating to the first and second units.

2. (Previously Presented) The apparatus of claim 1, wherein the first unit comprises a processor unit.

3. (Previously Presented) The apparatus of claim 1, wherein the second unit comprises a video processor unit.

4. (Previously Presented) The apparatus of claim 1, wherein the first unit comprises a hard disk drive controller unit.

5. (Previously Presented) The apparatus of claim 1, wherein the second unit comprises an isochronous data transfer unit.

6. (Cancelled)

7. (Previously Presented) The apparatus of claim 5, wherein the isochronous data transfer unit comprises a 1394 controller unit.

8. (Previously Presented) The apparatus of claim 5, wherein the isochronous data transfer unit comprises a USB controller unit.

9. (Cancelled)

10. (Currently Amended) A system comprising:

a device coupled to a variable speed bus, the device having a rate of request to access the variable speed bus; and

an arbitration and bus clock control unit to monitor the rate of request, and to determine a clock frequency associated with the variable speed bus based on the rate of request, ~~wherein~~ the arbitration and bus clock control unit being modified to track the rate of request to access the variable speed bus, the arbitration and bus clock control unit ~~is~~ being further modified to recognize when there are no incoming requests and a percentage of arbitration slots that are being used, and to instruct a clock throttling logic to adjust the clock frequency associated with the variable speed bus based on the rate of request to access the variable speed bus from the device, wherein the adjusting of the clock frequency includes lowering the clock frequency to a lowest level necessary in accordance with the recognition of no incoming requests and the percentage of the arbitration slots being used and further in accordance with a historical average utilization including statistical data relating to sustained bandwidth needs such that the clock frequency of the variable speed bus is automatically adjusted depending on one or more of the rate of request, the percentage of arbitration slots being used, and the historical average utilization relating to the first and second units.

11. (Cancelled)

12. (Previously Presented) The system of claim 10, wherein the device coupled to the variable speed bus comprises a processor.

13. (Previously Presented) The system of claim 10, wherein the device coupled to the variable speed bus comprises a video processor.

14. (Previously Presented) The system of claim 10, wherein the device coupled to the variable speed bus comprises a hard disk drive controller.

15. (Previously Presented) The system of claim 10, wherein the device coupled to the variable speed bus comprises an isochronous data transfer controller.

16. (Cancelled)

17. (Previously Presented) The system of claim 15, wherein the isochronous data transfer controller comprises a 1394 controller.

18. (Previously Presented) The system of claim 15, wherein the isochronous data transfer controller comprises a USB controller.

19-21 (Cancelled)

22. (Previously Presented) The system of claim 10, wherein the arbitration and bus clock control unit determines the second clock frequency based on a first bandwidth requirement from the first unit and a second bandwidth requirement from the second unit, the first bandwidth requirement derived from the first rate of request to access the variable speed bus from the first unit, the second bandwidth requirement derived from the second rate of request to access the variable speed bus from the second unit.

23. (Previously Presented) The system of claim 10, wherein the variable speed bus, the first unit, the second unit, the clock throttling logic and the arbitration and clock control unit are located on a single semiconductor die.

24. (Cancelled)

25. (Currently Amended) A method comprising:

initializing a variable speed bus with a first clock frequency;

accessing the variable speed bus by the first unit having a first rate of requests, the first unit coupled to the variable speed bus;

accessing the variable speed bus by the second unit having a second rate of requests, the second unit coupled to the variable speed bus; and

monitoring, by an arbitration and bus clock control unit, the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on the first access rate or the second access request rate, ~~wherein~~ the arbitration and bus clock control unit ~~is further~~ being modified to track a rate of request of the first and second units to access the variable speed bus, the arbitration and bus clock control unit ~~is~~ being further modified to recognize when there are no incoming requests and a percentage of arbitration slots that are being used, and to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request, wherein the adjusting of the clock frequency includes lowering the clock frequency to a lowest level necessary in accordance with the recognition of no incoming requests and the percentage of the arbitration slots being used and further in accordance with a historical average utilization including statistical data relating to sustained bandwidth needs such that the clock frequency of the variable speed bus is automatically adjusted depending on one or more of the rate of request, the percentage of arbitration slots being used, and the historical average utilization relating to the first and second units.

26. (Previously Presented) The method of claim 1, wherein the first unit comprises a processor unit.

27. (Previously Presented) The method of claim 1, wherein the second unit comprises a video processor unit.

28. (Previously Presented) The method of claim 1, wherein the first unit comprises a hard disk drive controller unit.

29. (Previously Presented) The method of claim 1, wherein the second unit comprises an isochronous data transfer unit.